IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Continuation of International Application No. PCT/FR99/02569

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Inventors: Didier Serra, Nicolas Pangaud, Michel Martin, and Francois Bergouignan

Title: *Contactless Integrated Circuit with Reduced Power Consumption*

Priority: French Application No. 98/13470; Filed 23 October 1998

Attorney Docket: 1400.005 Customer No. 023907

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Box Patent Application
Washington DC 20231

Sir:

This Preliminary Amendment is directed to the continuation application of International Application PCT/FR99/02569 as identified above. Please enter this preliminary amendment prior to calculating the fees.

IN THE SPECIFICATION

Page 1, after the title insert -- This is a continuation of International Application PCT/FR99/02569, with an international filing date of October 22, 1999. --

Page 1, before line 1, insert the heading -- BACKGROUND OF THE INVENTION --; and the subheading -- 1. Field of the Invention --;

Page 2, between lines 19 and 20, insert the subheading -- 2. Description of the Related Art --;

Page 4, between lines 2 and 3, insert the heading -- OBJECTS AND SUMMARY OF THE INVENTION --;

Page 5, between lines 26 and 27, insert the heading -- BRIEF DESCRIPTION OF THE DRAWINGS --;

Page 7, line 17, insert the heading -- DESCRIPTION OF THE PREFERRED EMBODIMENTS --.

IN THE CLAIMS

Please amend claims 3, 4, 6, 7, 8, 9, 10 and 11. Following are the claims as amended. A marked-up version of the changes made to the claims is attached and entitled *Version with Markings to Show Changes Made.*

3. (Amended) Integrated circuit according to claim 1, wherein the means (CC1) for delivering the pulsed modulation signal (Slm4) comprise at least two capacitors (Cref, Cas) and means (WLCC, CG1, CMP, D6, SR1, T1, T2, T3, T4) for:

- charging the first capacitor (Cref) with a constant current (Iref) before the emission of a load modulation pulse, during a time (Tref) fixed by a predetermined number of clock cycles (H),
- charging the second capacitor (Cas) with a constant current (Iref) during the emission of a pulse, and
- stopping the emission of the pulse when the charge voltage (Vas) of the second capacitor is equal to the voltage (Vref) at the terminals of the first capacitor.

4. (Amended) Integrated circuit according to claim 1, comprising means (WLCC) for:

- transforming the binary signal to be transmitted (DTx) into a binary coded signal (S1) presenting at least, at each bit of the binary signal, a rising or falling variation edge, and
- transforming variation edges of the binary coded signal (S1) into load modulation pulses (I1-In) of short duration compared to the duration (Tb) of a bit of the binary signal to be transmitted (DTx).

6. Integrated circuit according to claim 1, wherein the modulation signal (Slm4) is combined with an a.c. signal (Fsc) in order to form a load modulation signal comprising a.c. signal pulses.

7. Integrated circuit according to claim 1, wherein the load modulation pulses have a duration (Tas) shorter than or equal to the quarter of the duration of a bit of the binary signal to be transmitted (DTx).

8. Integrated circuit according to claim 1, wherein the clock extraction device (CEC1) is maintained in an inhibited state after the emission a load modulation pulse, at least for a time (Tref, Tas) equal to the duration of a load modulation pulse.

9. Integrated Circuit according to claim 1, wherein the clock extraction device (CEC1) is arranged to extract a clock signal (H) from an a.c. voltage (Vac) induced in the antenna coil (Ls).

10. Integrated circuit according to claim 1, characterized in that it comprises means (Pd, C2) for extracting a d.c. supply voltage (Vcc) from the a.c. voltage (Vac) induced in the antenna coil (Ls).

11. Integrated circuit according to claim 1, wherein the means for inhibiting the clock extraction device (CEC1) comprises means (T5, T6) for powering-off the extraction device (CEC1).

IN THE ABSTRACT

Please add page 22 containing an Abstract of the Disclosure.

REMARKS

The application has been amended to insert headings in the specification, to eliminate the multiple dependencies in the claims, and to add an Abstract of the Disclosure.

Entry of the amendments and examination of the continuation international application are respectfully requested.

Respectfully submitted,

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Date: April 23, 2001

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

3. (Amended) Integrated circuit according to [one of the claims 1 and 2] claim 1, wherein the means (CC1) for delivering the pulsed modulation signal (Slm4) comprise at least two capacitors (Cref, Cas) and means (WLCC, CG1, CMP, D6, SR1, T1, T2, T3, T4) for:

- charging the first capacitor (Cref) with a constant current (Iref) before the emission of a load modulation pulse, during a time (Tref) fixed by a predetermined number of clock cycles (H),
- charging the second capacitor (Cas) with a constant current (Iref) during the emission of a pulse, and
- stopping the emission of the pulse when the charge voltage (Vas) of the second capacitor is equal to the voltage (Vref) at the terminals of the first capacitor.

4. (Amended) Integrated circuit according to [one of the claims 1 to 3] claim 1, comprising means (WLCC) for:

- transforming the binary signal to be transmitted (DTx) into a binary coded signal (S1) presenting at least, at each bit of the binary signal, a rising or falling variation edge, and
- transforming variation edges of the binary coded signal (S1) into load modulation pulses (I1-In) of short duration compared to the duration (Tb) of a bit of the binary signal to be transmitted (DTx).

6. Integrated circuit according to [one of the claims 1 to 5] claim 1, wherein the modulation signal (Slm4) is combined with an a.c. signal (Fsc) in order to form a load modulation signal comprising a.c. signal pulses.

7. Integrated circuit according to [one of the claims 1 to 6] claim 1, wherein the load modulation pulses have a duration (Tas) shorter than or equal to the quarter of the duration of a bit of the binary signal to be transmitted (DTx).

8. Integrated circuit according to [one of the claims 1 to 7] claim 1, wherein the clock extraction device (CEC1) is maintained in an inhibited state after the emission a load modulation pulse, at least for a time (Tref, Tas) equal to the duration of a load modulation pulse.

9. Integrated Circuit according to [one of the claims 1 to 8] claim 1, wherein the clock extraction device (CEC1) is arranged to extract a clock signal (H) from an a.c. voltage (Vac) induced in the antenna coil (Ls).

10. Integrated circuit according to [one of the claims 1 to 9] claim 1, characterized in that it comprises means (Pd, C2) for extracting a d.c. supply voltage (Vcc) from the a.c. voltage (Vac) induced in the antenna coil (Ls).

11. Integrated circuit according to [one of the claims 1 to 10] claim 1, wherein the means for inhibiting the clock extraction device (CEC1) comprises means (T5, T6) for powering-off the extraction device (CEC1).